Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A command multiplier that generates sets of command, address, and data inputs (CAD) from a seed set having a plurality of bits provided at a low frequency by a BIST, to an embedded memory at a high frequency, comprising:
a directive register;
a logic unit; and
a multiplexer for time-multiplexing n generated CAD sets to the memory system at a frequency n times greater than the frequency at which the seed CAD set is received.

[c2] 2.The command multiplier of claim 1 wherein there are c directive registers corresponding to c seed CAD bits, each register having n directive bits corresponding to the n CAD sets to be generated; and
n logic units (LUs) corresponding to the n CAD sets to be generated, each LU taking as an input the i th bit of the seed CAD and one of the n bits from the i th directive register.

[c3] 3.The command multiplier of claim 1 wherein there are c directive registers corresponding to c seed CAD bits,

each register having n directive bits corresponding to the n CAD sets to be generated; and

n logic units (LUs) corresponding to the n CAD sets to be generated, each LU taking as an input the i th bit of the seed CAD, one of the n bits from the i th directive register, and the binary-encoded time interval, m.

[c4] 4.The command multiplier of claim 1 wherein there are c directive registers corresponding to c seed CAD bits, each register having n directive bits corresponding to the n CAD sets to be generated; and

n logic units (LUs) corresponding to the n CAD sets to be generated, each LU taking as an input the i th bit of the seed CAD, one of the n bits from the i th directive register, and a binary-encoded value corresponding to its directive bit input.

[c5] 5.A command multiplier that generates multiple sets of command, address, and data inputs (CAD) from a seed CAD set having a plurality of bits provided at a low frequency to a memory system at a high frequency, comprising:

c directive registers corresponding to c seed CAD bits, each register having one or more directive bits;

a logic unit (LU) taking as an input the i th bit of the seed CAD, all of the bits from the i th directive register, and a binary-encoded time interval, m; and

a multiplexer for time-multiplexing n generated CAD sets to the memory system at a frequency n times greater than the frequency at which the seed CAD set is received;

[c6] 6.A command multiplier that generates multiple sets of command, address, and data inputs (CAD) from a seed CAD set having a plurality of bits provided at a low frequency to a memory system at a high frequency, comprising:
a register;
an arithmetic logic unit (ALU); and
a multiplexer for time-multiplexing n generated CAD sets to the memory system at a frequency n times greater than the frequency at which the seed CAD sets are received.

[c7] 7.The command multiplier of claim 6 which includes address offset registers corresponding to the n CAD sets to be generated, each contents of which is added to the corresponding seed address by the ALU to generate one of the n output addresses.

[c8] 8.The command multiplier of claim 6 which includes opcode registers corresponding to the n CAD sets to be generated, each contents of which is combined with the corresponding seed CAD control signals to generate one

of the n of that control signal.

[c9] 9. A method for generating multiple sets of command, address, data inputs (CAD) from a seed CAD set having a plurality of bits provided by a BIST at low speed f_{BIST} to a memory system at a higher speed f_{MEM} comprising the steps of:

Loading a command multiplier register from the BIST;

ending the seed CAD set from the BIST to a logic block to generate n CAD sets; and

providing the n CAD sets to a multiplexer to send the CAD sets to the memory system at f_{MEM}.

[c10] 10. The method of claim 9 wherein the logic block is either a logic unit or an ALU.